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Development of FPGA based In-System-Programmable PWM Technique

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***Abstract*— The present paper is a Field Programmable Gate Array (FPGA) based system which is applicable for controlling the speed of electric motors, by means of varying the pulse width of an electric signal given to the motor. The system designed here is user friendly to vary the pulse width, and hence the motor speed; by just pressing the keys on a hex keypad. It does not require reconfiguration of the controlling device to vary the pulse width. The Soft Intellectual Proprietary (IP) Core was developed by instantiating two modules together and the top level Very High Speed Integrated Circuit Hardware Description Language (VHDL) entity was designed. In addition of two cores the source code was designed with having a process that permits the data entry from the keypad to the Pulse Width Modulation (PWM) unit. The Xilinx (Integrated System Environment) ISE Design Suit was used for the system design and the hardware implementation in the Spartan 3E FPGA device. The Digital Storage Oscilloscope (DSO) was deployed to observe and test the system that changes the pulse width of an output signal; in accordance with the key pressed on the hex keypad.**

***Keywords*— FPGA, Hex keypad, Motor Speed, PWM, Spartan 3E**

I. Introduction

Pulse Width Modulation (PWM), refers to the method of applying a square wave signal to an electric motor or a fan that varies its speed by changing the signal duty cycle. PWM is the preferred approach to regulating motor speed for the main reasons as given in [1].

A sinusoidal PWM technique suitable for single-chip microprocessor-based control is described in [2]. Its proposed scheme can be considered as a digital alternative to the conventional sub harmonic method in the sense that online real-time PWM control is possible and synchronization between carrier wave and signal wave is unnecessary. The scheme features a maximum output voltage that is 15% greater than for the sub-harmonic method, and the number of switchings is 30% less. A description of the PWM pulse-creation principle is also given in [2]. Most inverter loads have a low-pass filter nature. Taking this into account, a performance function (PF), which is the time-integral function of the inverter output voltage, is introduced. An optimal PWM pattern is obtained by minimizing the distortion factor of the PF. As the calculation of the optimal pattern needs only three multiplications, it can be executed online with a minimum read-only-memory capacity using a conventional microprocessor. The experiment was carried out with an Intel 8096 CPU. A Comparison of PWM Techniques and Inverter Performance reported in [3] shows that, the performance of the motor with the pulse (Space Vector PWM), SVPWM which is applied to inverter is better than TRAPEZOIDAL and SPWM.

Many digital techniques are based on the use of counter and comparator based design. These digital techniques are easier to implement than analogue techniques. Also they are immune to environmental noise and temperature change. The FPGA based PWM techniques for controlling Inverter has been reported in [4].

The present paper deals with development of an FPGA based PWM technique, in which the pulse width is programmable in run-time. That means the output square wave pulse-width is variable without requirement of any further programming; once the FPGA device is hardwired. The pulse-width is variable just by pressing a key available on the keypad. The minimum duty cycle is programmable by pressing the key-1. Contrast to this, the maximum pulse-width is achievable by pressing the key-F. A clock source of 50MHz, available on the FPGA board was divided to get 350 KHz frequency at the output line; whose duty cycle was programmed in real time operations. The variations in the 'ON' time of the square-wave were observed in the range of 76 microseconds to 163 milliseconds; by inputting key-1 to key-F on the hex keypad. The pressed key was also displayed on the seven segment display, available on the Xilinx Spartan 3E FPGA board: Nexys2 developed by Digilent Inc..

II. Soft IP Core Development for Programmable PWM System

The PWM signal was generated using a counter that increments periodically (it was connected to the clock on the board i.e. 50MHz) and that resets at the end of every period of the PWM signal. When the counter value was more than the reference value, the PWM output was changing the state from high to low. The PWM module generates the PWM signal using the clock input and an 8-bit input 'cmpPwm'.

'CmpPwm' is a reference value which compare with the internal counter value. When cmpPwm = 0 the pulse width was minimum (output LOW), and when 'cmpPwm' = 255 the pulse width was maximum (output HIGH). The pulse width was proportional to the reference value [5].

In this reference component as given in [5], the input reference values were provided at its 8 bit input lines. However, in the present research work these values were supplied from the hex keypad, having '0' through 'F' keys. The hex keypad driver module given in [6] was used in this work. These two modules were instantiated together to form a new and top level Very High Speed Integrated Circuit Hardware Description Language (VHDL) module. The 8 bit data from the keypad output was entered in this top level entity by de-asserting the Reset signal, and asserting another input named as 'ACCEPT_T' at every positive transition event on the clock source. The keypad data was stored in an internal signal; connected to the input vector signal of PWM module. The entity structure of the top level module formed by combining PWM module and Keypad Driver module is shown in following lines of VHDL code.

```
entity PWM_V2F_KEYPad is
Port    ( ck_T :in  STD_LOGIC;
cmpPwm_T : in  STD_LOGIC_VECTOR(7 downto 0);
      pwm_out_T :      out  STD_LOGIC;
      RESET_T: in STD_LOGIC;
      ACCEPT_T :in STD_LOGIC;
      JA_T : inout  STD_LOGIC_VECTOR (7 downto 0);
      an_T : out  STD_LOGIC_VECTOR (3 downto 0
      seg_T : out  STD_LOGIC_VECTOR (6 downto 0));
end PWM_V2F_KEYPad;
```

The input signal 'cmpPwm_T' is given to the 8 bit output lines of key pad driver module. The output waveforms were observed on the Digital Storage Oscilloscope (DSO) by connecting its channel to the output signal, 'pwm_out_T'. A global clock and reset signals were provided at the input signals named as 'ck_T' and 'RESET_T', respectively. The 'ACCEPT_T' signal controls the entry of keypad generated signals and allows getting in this top level entity; when it is asserted high.

The Keypad driver core was stimulated by keypad-generated 8 bit data, and the same signal was also given to the PWM module. These two signals were commonly connected and given to the top level entity. This common signal is named as 'JA_T'. The number associated with the key-press was also displayed on the seven segment displays; available on the Nexys2 FPGA board. The board has four such displays, however to glow segment LEDs (light emitting diodes) the particular display (of common anode type) has to be enabled. For that the output signal called as 'an_T' was engaged. To glow the least significant display (out of 4) this signal was generating "0001" output. The selected display's segment data was provided on 7 bit output signal, 'seg_T'.

To perform the 'port map' operations and interconnect two modules together, the following VHDL construct of an architecture designing was developed.

```
U_PWM: PWM
      port map (ck => ck_T,
                  cmpPwm => pwm_out_T_int,
                  pwm_out => pwm_out_T );
U_PmodKYPD: PmodKYPD
      port map (clk => ck_T,
                  JA => JA_T,
                  an => an_T,
                  seg => seg_T );
```

This architecture also has a process (shown below) executing to accept the 8 bit data from the keypad, and route it further as an input to the PWM module. The PWM module changes the width of the output signal-waveform; according the magnitude of the data coming from the keypad.

```
process (ck_T, RESET_T)
begin
   if RESET_T='1' then
      pwm_out_T_int<= (others=>'0');
   elsif rising_edge(ck_T) and (ACCEPT_T='1') then
      pwm_out_T_int<= JA_T;
   end if;
end process;
```

III. Synthesis Results of the In-System-Programmable PWM Soft IP Core

The Fig.1 shows a Register Transfer Level (RTL) view of the synthesis results, obtained in Xilinx ISE (Integrated System Environment) design flow, of version 14.6.

The internal view of the top level VHDL Soft IP Core is shown in Fig.2, which illustrates the interconnections of two modules.

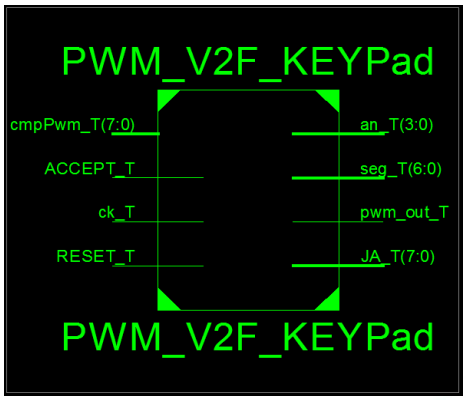

Figure 1. RTL Synthesis view of Top Level RTL View of the System.

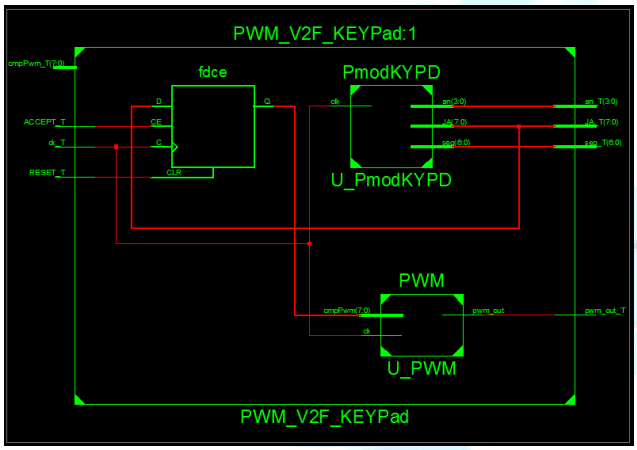

Figure 2. A Detailed View of the Top Level Entity with three sub modules instantiated together

The Fig.2 shows three modules interconnected together. The module named as 'PmodKYPD', drives the hex keypad, and the 'PWM' module generates a square wave; in accordance with the input data available from output of third module named as 'fdce'. Because of a process introduced in the architecture, this new module ('fdce'), which was not the part of structural modelling style used in VHDL architecture, has now become one of the modules in the internal view of RTL synthesis. The Table I gives the details of the project status with the device and project details.

TABLE I. PROJECT STATUS FOR THE SYSTEM

PWM_V2F_KEYPad Project Status (10/07/2013 - 06:11:10)			
Project File:	PWM_VtoF.xise	Parser Errors:	No Errors
Module Name:	PWM_V2F_KEYPad	Implementation State:	Programming File Generated
Target Device:	xc3s500e-4fg320	Errors:	No Errors
Product Version:	ISE 14.6	Warnings:	1 Warning (0 new)
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	All Constraints Met
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

The Table II gives the device utilization summary and shows the percentage wiz FPGA resources utilization.

TABLE II. DEVICE UTILIZATION SUMMARY

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	50	9312	1%
Number of 4 input LUTs	110	9312	1%
Number of occupied Slice	78	4656	1%
Total Number of 4 input LUTs	144	9312	1%
Number of bonded IOBs	23	232	4%
Number of BUFGMUXs	1	24	4%

IV. Hardware Implementation and Generating PWM Waveforms

After configuring the FPGA device embedded on Nexys2 board, the keypad was attached to the Pmod connector, 'JA' on the board. The output square wave was taken from 'JB1' pin of the Pmod connector, 'JB' and connected to the DSO channel. It was observed that, by pressing different keys on hex keypad, the pulse width of the output signal was changing. The key-press was started from key-1 and last output waveform was noticed by key-F from the keypad. The Table III shows some pressed keys for which the positive width of waveforms generated at the output. It shows that, there is almost linear proportionality between the 8 bit input data and pulse width.

TABLE III. PULSE WIDTH VARIATIONS AS PER KEYS PRESSED ON HEX KEYPAD

Key	1	2	3	4	5	…	E	F
PW (µsec)	76	78	80	117	120	…	162	163

The few photographs of waveforms observed on DSO, for different keys are given in Fig. 3. It shows the output pulse width of 76 microseconds; when the key-1 was pressed. Consequently, when key-2 was pressed it generate the positive signal pulse width of 78 microseconds. The photograph taken at the time of actual testing of the system shows the waveform of the pulse width of order of 163 microseconds; when key-F was pressed.

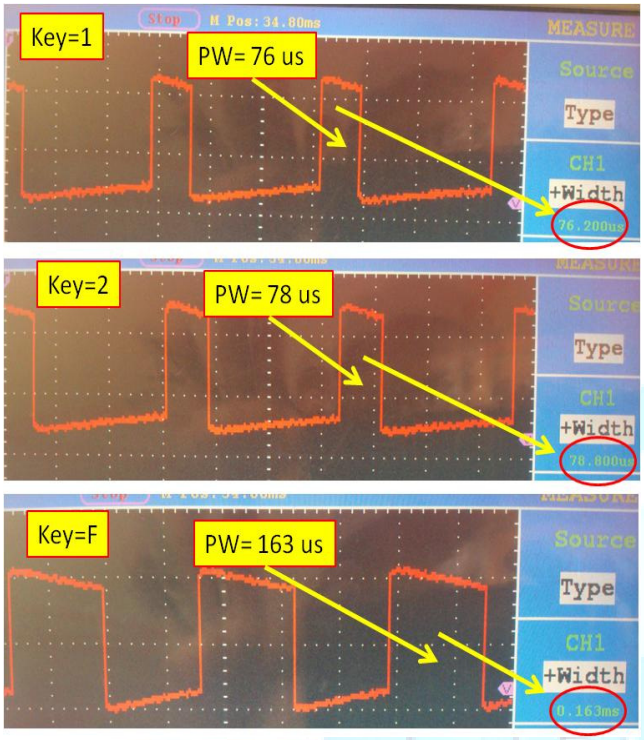

Figure 3. Waveforms generated for Keys: 1, 2 and F on Hex Keypad, observed on Digital Storage Oscilloscope (DSO)

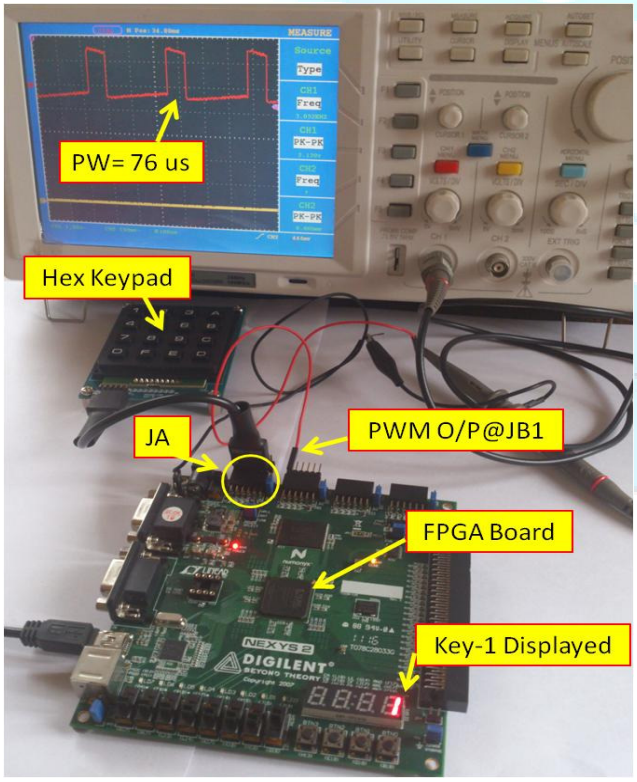

Figure 4. Experimental Setup for Run-time Programmable PWM System assembled with Hex Keypad and FPGA Board and DSO

The complete experimental setup developed for real time testing is shown in Fig. 4. It shows an FPGA board Nexys2, developed by Digilent Inc. The detail of the interfacing and various on-board facilities are given in [7]. It also shows a hex keypad interfaced with FPGA board by interconnecting it with Pmod connector, JA. The DSO channel is shown; connected to the output signal emerging from FPGA line constrained to Pmod connector pin, JB1.

The Fig.4 also shows the displayed number on a seven segment display; corresponding to the key pressed on the hex keypad. The DSO channel also shows the pulse width of the order of 76 microseconds; when key-1 was pressed on the keypad.

Conclusion

The present research work shows the ways of generating different pulse widths by just hitting the keys available on a hex keypad. The key pad provides binary data to the PWM-generating module that accepts the data as a reference value, up to which its internal counter reaches and then toggles the output signal. Simultaneous to this it also portrays display of the corresponding key-pressed; in accordance to which the FPGA generates a pulse width. Such a system has its wide applications to control the electric motors; installed in various embedded system. The future development of this project work could be extended to use the Personal System, PS/2 keyboard, and generate more pulse widths than the possible with the hex keypad.

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